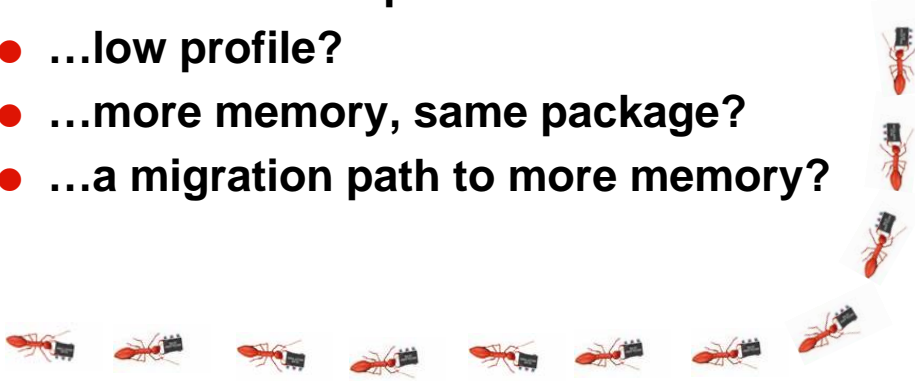


Tiny EEPROM Packages: More choices than the SOIC

Do You Need...

- ...a smaller footprint?
- ...low profile?
- ...more memory, same package?
- ...a migration path to more memory?



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EEPROM Packages

Slide 1

Welcome to the latest in Microchip's series of web seminars about serial EEPROMs. I'm Barry Blixt, marketing manager for Microchip memory products. We'll spend the next 15 minutes discussing some of the newer small package options that are now available for Microchip EEPROMs.

For years, the most popular package for serial EEPROMs has been the 8-lead small outline, or SOIC, package. In fact, it is basically the industry-standard package.

But, two things have happened over the last few years that have made other, smaller package options more popular. First, embedded designs have moved into more and more applications, many with severe space constraints. So, the demand for small packages has increased. Second, as silicon technologies have evolved, die sizes have shrunk, and larger density memories have become available in smaller packages.

So, do you need smaller packages? Are you looking for other options besides the SOIC? Here are some other questions to think about:

Do you have a footprint-limited design that would benefit from smaller packages?

Do you have height constraints in a low-profile application?

Do you have a current design that requires more memory, but you can not change the physical layout?

Finally, are you looking for a migration path to more memory?

If you face any of these problems, this web seminar will be helpful as we will be looking at specific small-package solutions.



Agenda:

- **EEPROM review**
- **Package summary**
- **Density vs. package**
- **Die and wafer**



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Here is our agenda for this seminar:


We'll start out with a brief review of serial EEPROMs, their advantages, and why they are so widely used.

The major portion of this seminar will be a summary of the current packages that are available, along with their footprint and height dimensions. Along with that, I'll offer some specifics about choosing the optimum package.

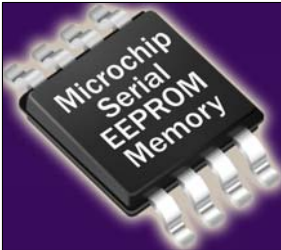
This will lead into a summary of the maximum amount of memory, or density, that is available in each package.

We'll finish up with a look at the strengths and weaknesses of the ultimate in small packages: bare die and wafers.

With that, let's take a look at the advantages of EEPROMs.



EEPROM Features



Low current & power

**1.7 to 5.5V,
- 40 to 125°C**

128 b – 1 Mb

3 bus types

**1,000,000
erase cycles**

PACKAGING OPTIONS

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Designers use serial EEPROMs in many embedded applications where non-volatile memory is required to store calibration data, logged data, or other permanent information. On this slide, we'll look at a quick summary of some of the advantages of EEPROMs, or E2's. For a more detailed explanation of the basics of EEPROMs, including discussions about the different advantages of each bus protocol, see Microchip's web seminar entitled "Serial EEPROM Overview." Later on, I'll show you where you can find these other web seminars on our web site.

First, serial EEPROMs are available in a wide range of densities, from 128 bits all the way up to 1 megabit.

Second, it is very easy to design with EEPROMs and to interface them with a microcontroller or ASIC since E2s are available in 3 well-established bus protocols: I2C™, SPI, and Microwire.


EEPROMs are also well-known for their endurance characteristics. Under most conditions, an E2 can be written to and erased millions of times, well above the capacity of other non-volatile memory technologies. For a complete discussion on endurance, see our web seminar entitled, "Serial EEPROM Endurance."

Also, serial EEPROMs can be used over a wide voltage range - 1.7 to 5.5 volts - and a wide temperature range: all the way up to 125 degrees C. This is in contrast to flash-type memories that are usually only good from 2.5 to 3.6 volts and only up to 85 degrees C.

Finally, EEPROMs also have very low current draw in both operational and standby modes, so they are excellent for use in battery-powered applications.

In addition, EEPROMs are known for their byte-level operability, low pin counts, and low cost.

But another, often overlooked, feature of an EEPROM is the wide range of small packaging options that are available. In fact, the last couple years have brought several new packages to the EEPROM market that allow designers flexibility in their designs. Let's look at some package details.




EEPROM Packages				
Package		Footprint (mm)	Height (mm)	Max. Density (Kb)
SOIC		6 x 5	1.75	512

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On this slide, I'll be showing some package photos along with footprint and maximum height data. By footprint, I mean the total area that the package takes up, including pins. And although the package photos on this page are not to scale, the relative sizes are correct. I'll also list the maximum amount of memory that will fit into each package. And, I'll mention the relative price levels, since some packages are more expensive than others.

For example, let's look at the 8-lead SOIC. You will also see this package referred to as the JEDEC 150 mil SOIC. As I mentioned earlier, the SOIC package is the most popular package for EEPROMs. Its advantages are its relatively small footprint of 6 x 5 mm and the fact that virtually every EEPROM manufacturer makes it, so multiple sourcing is possible. You can see that is also fairly thin, at 1.75 mm high. Just about every density from 128 bits to 512 Kbits is available in this package, so it is easy to increase the amount of memory on a board without making any physical changes. And, it is one of the least expensive packages to manufacture.

But, what if you need more memory in a 6 x 5 mm area? Or, what if you need a lower profile package? That is where the 6 x 5 DFN, or dual flat no-lead package, can be useful.






 EEPROM Packages				
Package		Footprint (mm)	Height (mm)	Max. Density (Kb)
SOIC		6 x 5	1.75	512
DFN		6 x 5	1.0	1024

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The 6x5 DFN has the same footprint and landing pattern as the SOIC. This slide shows photos of both the top side and the underside of the DFN. I've lined up the photos so that the SOIC package is just above the underside of the DFN. You can see that the two parts have the same footprint and that all eight leads are lined up.

But notice how much bigger the black plastic molding compound is on the DFN. Since the leads are tucked underneath, there is room for a larger die to fit into the package. In fact, we can fit our new 1 Mbit die into this package, and still maintain the footprint of the SOIC package. That helps with keeping board size smaller and also means there is a migration path in this footprint all the way from 128 bits to 1 Mbit. This package also has a very low profile of 1 mm, so it is excellent for applications needing a large amount of memory in a short space. Like all advanced, leadless packages, the DFN is more expensive than the SOIC.







Now, what if you need a smaller footprint than the two 6x5 mm packages we just discussed, but you still want an industry-standard package? These next two packages could provide the answer.

 EEPROM Packages				
Package		Footprint (mm)	Height (mm)	Max. Density (Kb)
SOIC		6 x 5	1.75	512
DFN		6 x 5	1.0	1024
TSSOP		3 x 6.4	1.2	256
MSOP		3 x 4.9	1.1	256
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The 8-lead TSSOP, or Thin Shrink Small Outline Package, and the 8-lead MSOP, or Micro Small Outline Package, are very similar. Both have the same width of 3 mm and a height of just over 1 mm; both have the same distance, or pitch, between their pins. Both can hold up to 256 Kbits of memory. And, both are typically more expensive than the SOIC.








There are two major differences. First, the MSOP is about 25% shorter at 4.9 mm. Second, the MSOP is a bit less expensive to build. So while the TSSOP package is the more common option, the MSOP package is a good alternative. Many customers lay out their boards to accept both packages in order to take advantage of the MSOP's cost benefits.

Now, what if you need an even smaller package and system cost is crucial? Let's look at the SOT-23.

<div> EEPROM Packages</div>				
Package		Footprint (mm)	Height (mm)	Max. Density (Kb)
SOIC		6 x 5	1.75	512
DFN		6 x 5	1.0	1024
TSSOP		3 x 6.4	1.2	256
MSOP		3 x 4.9	1.1	256
SOT-23		3.2 x 3.1	1.45	16
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The SOT-23 package shown here is just over 3 x 3 mm square. In fact, it is really a transistor package available in 5-lead and 6-lead options. It is available in densities up to 16 Kbits. Its price is on par with the SOIC, so it represents a good value in a small space.

Microchip also has a series of microcontrollers and many analog parts in the SOT-23 package. So, you could actually create a complete system using nothing but tiny SOT-23 packages.

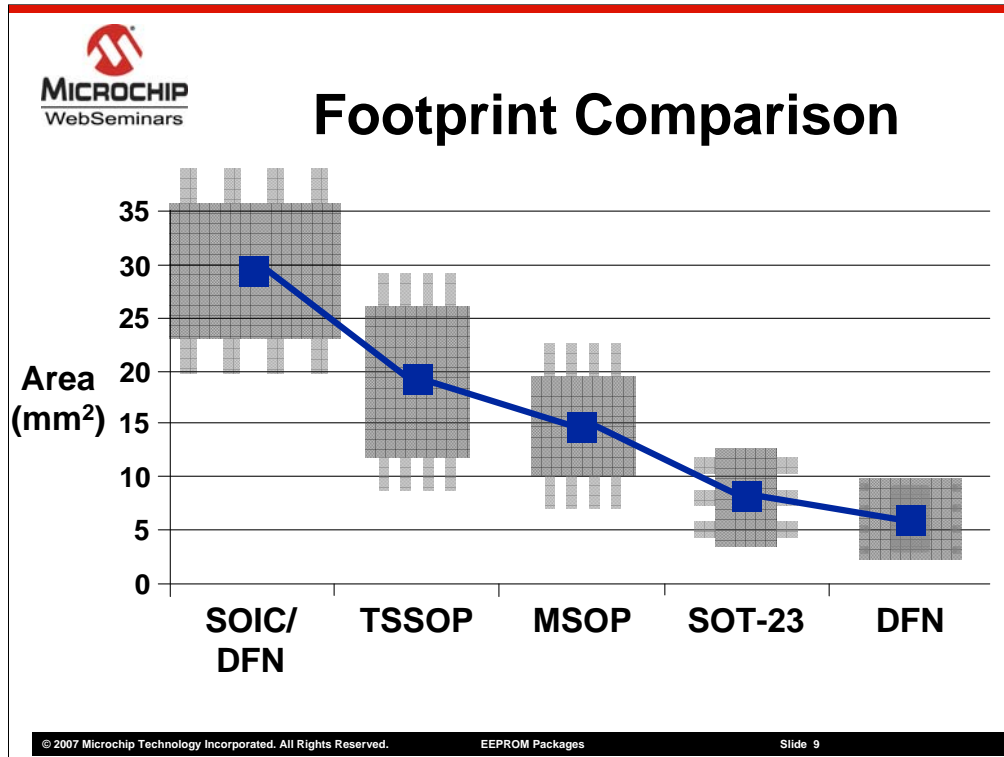
 <h2>EEPROM Packages</h2>				
Package		Footprint (mm)	Height (mm)	Max. Density (Kb)
SOIC		6 x 5	1.75	512
DFN		6 x 5	1.0	1024
TSSOP		3 x 6.4	1.2	256
MSOP		3 x 4.9	1.1	256
SOT-23		3.2 x 3.1	1.45	16
DFN		2 x 3	1.0	64
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The smallest package on the market is the 2 x 3 mm DFN, another 8-lead dual flat no lead package. It has the smallest footprint, as well as the shortest height. And it is leadless, so a fairly large die can fit inside the package. Microchip has up to 64 Kbit devices in the 2x3 DFN. Its drawback is that like other leadless packages, it is more expensive to manufacture.

The SOT-23 and 2x3 DFN packages are the smallest EEPROM packages available today. They are so small that many designers, who may not have an immediate need for external memory, actually lay out the lands and leads for an extra package on the board. So, if it turns out that they need some extra memory, there is a small bit space reserved on the board.

You don't have to memorize the data on this slide. Later on, I will tell you how you can download Microchip's MAPS software tool that is an easy way to tell which densities are available in which packages.

One other comment about this chart. I have not shown PDIP packages, since those through-hole packages are so much larger than the surface-mounted ones I've discussed here. Microchip continues to offer PDIPs in all our devices.



This slide shows another way to look at the footprints of these packages.

The graph will show the area that each of these packages takes on a board. The y-axis shows the footprint of each package in square millimeters. Each package type is shown along the x-axis. For example, you can see that the blue square currently on the chart is just below 30 sq. mm., meaning that the SOIC and DFN packages in the first column have a footprint of just under 30 sq. mm. In the background, I've added an outline of the SOIC package.

Remember that the TSSOP and MSOP packages are very similar, with the same width and pin pitch. You can see on the chart that the TSSOP package has a footprint of about 19 sq. mm. and the MSOP is about 15 sq. mm., both quite a bit smaller than the SOIC.

The SOT-23 and 2x3 DFN packages, that I've just added to the chart, are both well under 10 sq. mm., which is less than a third of the area of the SOIC. Again, the package drawings are not to scale, but they are correct relative to each other.

This visual really dramatizes how small some of these packages are, especially when compared to the industry's de facto standard, the SOIC.



Need Even Smaller?

- **Unpackaged die and wafer**
 - 😊 **Small size**
 - 😞 **Storage and assembly**
- **Almost all EEPROMs available in die**
- **Thickness options**
- **3 format options**
 - **Unsawn wafer**
 - **Sawn wafer on frame**
 - **Die in waffle pack**



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As we have just seen, the 2x3 DFN and the SOT-23 packages are very small. But, what if you need something even smaller? That's when you can think about using bare die. This form factor is very popular in smart cards as well as in dual-die solutions with an ASIC or hybrid.

The advantage of using die is that it represents the smallest available form factor. It is also a good way to bond an EEPROM to another die within a single package. The disadvantage of using die is that handling bare die requires specialized knowledge and equipment. Even die storage can be tricky, since it requires special conditions.

But, we have many customers who buy die from us, and we make it easy to do so. Virtually all Microchip EEPROM products are available in die. We offer die and wafers in a variety thickness.

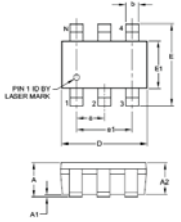
We also offer die in 3 formats: unsawn wafer, sawn wafer on a frame with sticky tape, and pre-cut die packed in a special shipping box called a waffle pack.

Another issue with die sales is that, unlike packaged parts which have standard dimensions, die layouts are different for each manufacturer. So, once a designer chooses a die supplier, that die effectively becomes sole-sourced. So, the designer ultimately needs to be able to count on both short-term and long-term supply. Our many die customers appreciate Microchip's history of stable supply and long product life cycles. Contact your local MCHP sales representative to get more information on die and wafer sales.



For More Info

- **MAPS**
Microchip Advanced Product Selector
www.microchip.com/MAPS
- **Packaging Specification**
www.microchip.com/packaging
- **Other EEPROM Webinars**
 1. **Overview** (27 Sept '05)
 2. **SEEVAL® 32 kit** (20 Oct '06)
 3. **Endurance** (31 Jan '07)



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EEPROM Packages


Slide 11

We have more information available on the web.

First, I encourage you to download our software-based product selection tool, called the Microchip Advanced Product Selector, or MAPS. It's available on our website. It includes Microchip's memory, microcontroller, and analog product lines. For memory parts, it is a simple way to find out which products are available in which packages. It also includes competitive information so you can find the correct Microchip EEPROM to replace a competitive device. The parametric search tool makes it extremely useful for selecting the optimum microcontroller, memory and analog components for your application. You enter the features you need, and MAPS tells you which devices meet your requirements. Just go to www.microchip.com/maps.

We have a very useful Packaging Specification on our web site as well. This document shows the package dimensions of all Microchip products. You can find this at www.microchip.com/packaging.

Finally, we have many more web seminars available, including 3 more on EEPROMs. You'll find an overview on serial EEPROMs, an introduction to our SEEVAL® memory development kit, and a tutorial on EEPROM endurance. I've listed the publish dates for each seminar to make them easier to find.



Summary of Key Points

1. **6x5 DFN and SOIC: same footprint**
2. **Consider the MSOP**
3. **SOT-23 value & SOT-23 micros**
4. **Save space for a tiny package**
5. **Bare die**

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We've talked about a lot in this presentation, so here's a chance to summarize some of the hints that I've mentioned throughout this talk.


First, remember that the 6x5 DFN and the industry-standard SOIC packages have the same footprint. That means there is a simple migration path to larger density parts.

Second, consider the MSOP package instead of the TSSOP package. It is smaller and can be less expensive.

Three, remember that the SOT-23 offers a very small package at a similar price point as the SOIC. And, Microchip small packaging leadership is not limited to EEPROMs. Microchip also offers the PIC10F family of microcontrollers in the SOT-23 package.

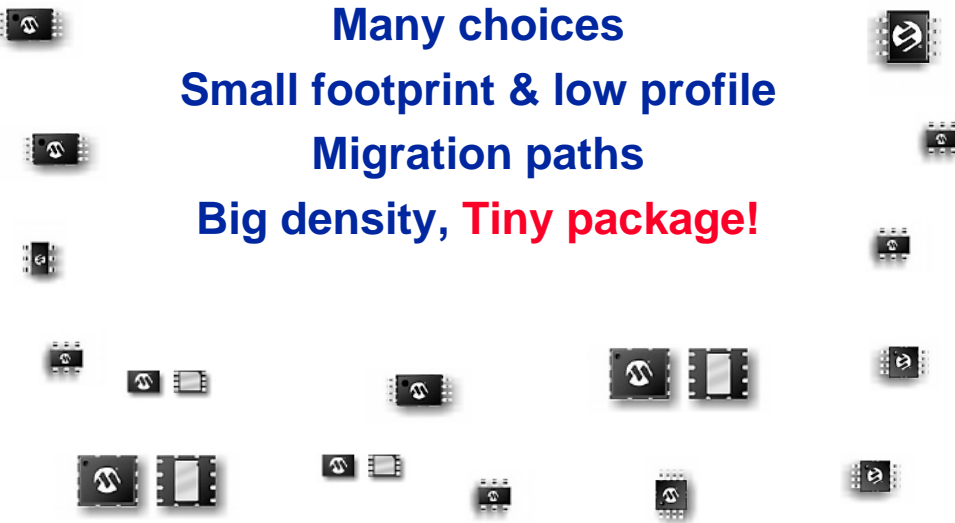
Fourth, some of these packages are so small that it might make sense to layout your board for a spare SOT-23 or 2x3 DFN package for future upgrades or bug fixes. It could save you a board spin if you find you need to add some extra memory - or even a microcontroller.

Finally, we just talked about die and wafer options. These can be excellent solutions in dual-die or space constrained applications.



Small EEPROM Packages

Many choices
Small footprint & low profile
Migration paths
Big density, Tiny package!



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And that concludes this web seminar on small package options for EEPROMs. To summarize, Microchip offers many different small package options in many different densities.

We supply packages with both small footprints and low profiles for the increasing number of applications that have space constraints.

Our package offerings allow migration paths to bigger densities since so many densities can fit into each package.

Finally, these package options allow you to fit a large amount of EEPROM memory in a small space to meet the demands of ever decreasing space allotments.

Thanks for your time.